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~~RCE 7/11/84~~

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March 7, 2005

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Gayle W Chaney
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*CHRIS PERKINS, PH.D.

Re: U.S. Patent Application Serial No. 10/050,341 for
DATA PROCESSING METHOD
Our File No. 1406/39

JEFFREY CHILDERS, PH.D.

THEODOSIOS THOMAS

OF COUNSEL
SOROJINI BISWAS

*LICENSED ONLY IN CA

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Sir:

Please find enclosed the following:

1. Request for Continued Examination (RCE) Transmittal (1 pg);
2. Copy of Amendment B filed 1/31/05;
3. A return-receipt postcard to be returned to our offices with the U.S. Patent and Trademark date stamp thereon; and
4. A Certificate of Express Mail No.: EV 611 690 585 US.

Please contact our offices if there are any questions with respect to this matter.

Commissioner for Patents
March 7, 2005
Page 2

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Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.



Richard E. Jenkins
Registration No.: 28,428

REJ/gwc

Enclosures

Customer No: 25297

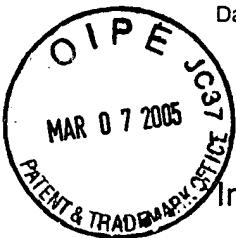
1406/39

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Gayle W. Charney
Gayle W. Charney
Date of Signature January 31, 2005

COPY **PATENT**

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Christian Panis

Group Art Unit: 2111

Serial No.: 10/050,341

Examiner: Kenneth S. Kim

Filed: January 16, 2002

Docket No.: 1406/39

Confirmation No.: 6236

For: DATA PROCESSING METHOD

AMENDMENT B

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is responsive to the Official Action dated December 13, 2004, for which a shortened statutory period for reply is set to expire on March 13, 2005. Favorable consideration is respectfully requested in view of the following Amendments and Remarks.

IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A data processing method using a multiplicity of processors which operate in parallel and to which a respective command for data processing is supplied simultaneously, at least one of the processors being alternatively supplied with ~~a program flow control command or~~ a condition command, the supplying of the condition command ~~deactivating conditioning~~ the parallel execution of a ~~further command in at least one of the further processors~~ all of the commands for data processing.
2. (Previously Presented) The data processing method as claimed in claim 1, wherein the supplying of the condition command has the effect that the computational result of one of the processors is not written back into a target register which is provided.
3. (Previously Presented) The data processing method as claimed in claim 1, wherein the supplying of the condition command has the effect that an address for the parallel executing of the further command is not calculated.
4. (Previously Presented) The data processing method as claimed in claim 1, wherein the supplying of the condition command has the effect that a command is not executed by the at least one of the further processors.
5. (Previously Presented) The data processing method as claimed in claim 1, wherein the further commands comprise arithmetic computational commands and/or move commands.

6. (Previously Presented) The data processing method as claimed in claim 1, wherein the condition which is associated with the condition command is the same for all of the further processors.

7. (Previously Presented) The data processing method as claimed in claim 1, wherein the condition which is associated with the condition command is different from all the further processors.

REMARKS

I. Status Summary

Claims 1-7 are currently pending. Claim 1 is amended herein. Therefore, upon entry of this Amendment, Claims 1-7 will be pending.

Element (b) of Claim 1 has been amended to include the phrase "wherein the base address register is switched through by the first multiplexer circuit". Support for the amendment to Claim 1 can be found throughout the subject application, particularly at page 5, lines 15-25, and page 5, line 36, to page 6, line 5.

II. Claim Rejections Under 35 U.S.C. § 102

Claims 1-7 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,287,465 to Kurosawa et al. (hereinafter, "Kurosawa"). This rejection is respectfully traversed.

Upon careful consideration and review of Kurosawa, applicant respectfully submits that Kurosawa does not disclose each and every element of amended Claim 1 and therefore does not anticipate the claim. Claim 1 recites a data processing method using a multiplicity of processors which operate in parallel and to which a respective command for data processing is supplied simultaneously. Further, Claim 1 has been amended to recite that at least one of the processors is supplied with a condition command which conditions the parallel execution of all the commands for data processing. Summarily, Kurosawa does not disclose that the commands for

data processing and the condition command are supplied simultaneously to a multiplicity of processors, or that the condition command conditions the parallel execution of all the commands for data processing, as required by Claim 1.

Kurosawa teaches a parallel processing apparatus comprising a program counter for indicating an instruction to be read out, m instruction registers for storing indicated instructions therein, arithmetic units sharing the register file and executing an arithmetic operation, plural instructions parallel processing means for reading consecutive instructions from an address indicated by the program counter, conditional branch instruction processing means. (Kurosawa, column 4, line 61, to column 5, line 3.) The condition branch instruction processing means has a condition branch instruction and an unconditional branch instruction. (Kurosawa, column 5, lines 3-5.) In this configuration, m instructions are first read out and decoded to check if there is a branch instruction in the k -th instruction. (Kurosawa, column 5, lines 16-19.) Further, Kurosawa teaches that first to $(k+1)$ th instructions are executed if the k -th instruction is a branch instruction. (Kurosawa, column 5, lines 16-34.) Referring to lines 22-25 of column 20, Kurosawa teaches that, at least with the branch instruction, the next instruction is executed irrespective of the satisfaction or nonsatisfaction of a condition. Thus, Kurosawa fails to teach that all commands for data processing are conditioned by the condition command, as required by Claim 1.

Further, Kurosawa teaches that the execution of the $(k+2)$ th to the m -th instructions is prevented if there is a branch instruction in the k -th instruction. (Kurosawa, column 5, lines 16-22.) If the condition fails, it remains unclear whether

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these last instructions are executed in parallel with the first instructions. In addition, the figures of Kurosawa suggest that the (k+2)th to the m-th instructions will always be executed after the k-th and the (k+1)th instructions, not in parallel. Applicant respectfully submits that nowhere does Kurosawa teach that a condition command conditions the parallel execution of all the commands for data processing, as required by Claim 1. Thus, Kurosawa cannot anticipate Claim 1. Applicant therefore respectfully submits that the rejection of Claim 1 under 35 U.S.C. § 102(b) be withdrawn and the claim allowed at this time.

Claims 2-7 depend from Claim 1. Therefore, Claims 2-7 includes the features of Claim 1. Thus, the comments presented above relating to Claim 1 apply equally to Claims 2-7. Therefore, Claims 2-7 are believed to be patentably distinguished over Kurosawa. Applicant respectfully requests that the rejections of Claims 2-7 under 35 U.S.C. § 102(b) be withdrawn and the claims allowed at this time.

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CONCLUSION

In light of the above amendments and remarks, it is respectfully submitted that the present application is now in proper condition for allowance, and an early notice to such effect is earnestly solicited.

If any small matter should remain outstanding after the Patent Examiner has had an opportunity to review the above Remarks, the Patent Examiner is respectfully requested to telephone the undersigned patent attorney in order to resolve these matters and avoid the issuance of another Official Action.

DEPOSIT ACCOUNT

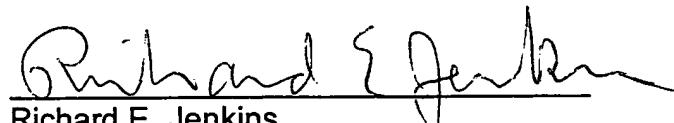
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Respectfully submitted,

JENKINS, WILSON & TAYLOR, P.A.

Date: January 31, 2005

By:


Richard E. Jenkins
Registration No. 28,428

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1406/39